IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Jae-Bon KOO

Serial No.:	10/764,525	Examiner:	*To be assigned*
Filed:	27 January 2004	Art Unit:	2673

For: FLAT PANEL DISPLAY WITH ANODE ELECTRODE LAYER AS POWER SUPPLY LAYER AND FABRICATION METHOD THEREOF

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. §1.56, and §§1.97 and 1.98 as amended, Applicant cites, describes, and provides copies of the following art references. Under 37 C.F.R. §1.98(a)(2) however, copies of U.S. patent reference(s) are not provided.

FOREIGN PATENT REFERENCE:

- Japanese Patent Publication No. 2003-15548 to Nozawa, *et. al.*, entitled *METHOD FOR MANUFACTURING ORGANIC EL DISPLAY BODY, METHOD FOR ARRANGING SEMICONDUCTOR DEVICE, METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE, METHOD FOR MANUFACTURING OPTOELECTRONIC DEVICE, OPTOELECTRONIC DEVICE, AND ELECTRONIC EQUIPMENT*, published on 17 January 2003 (with English abstract).

OTHER DOCUMENTS:

- Korean Office action for Korean patent application No. 10-2003-0007288 issued on 20 April 2005.

DISCUSSION

According to the Korean Office action, **Nozawa, *et al.* JP'548** discloses that many pieces of units, having fine structure, are formed in parallel on a silicon wafer. This unit has drive elements (a switching transistor 34, a drive transistor 37, a capacitance 36) of an organic EL element (pixel) 37. Then, unit blocks 39 are manufactured by dividing this silicon wafer. These unit blocks 39 are arranged at prescribed positions of a glass substrate (substrate for display) 52. Driving elements for respective pixels 35 are connected with signal lines 31, power source lines 32, scanning lines 33 and capacitance lines 38.

The citation of the foregoing references is not intended to constitute an assertion that other or more relevant art does not exist. Accordingly, the Examiner is requested to make a wide-ranging and thorough search of the relevant art.

No fee is incurred by this Statement.

Respectfully submitted,

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INFORMATION DISCLOSURE STATEMENT PTO-1449 (PAGE 1 OF 1)	SERIAL NUMBER 10/764,525	DOCKET NO. P56937
	APPLICANT Jae-Bon KOO	
	FILING DATE 27 January 2004	GROUP 2673

U.S. PATENT DOCUMENTS

EXAMINER	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE

FOREIGN PATENT DOCUMENTS — **TRANSLATION**

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	YES	NO
	JP 2003-15548	01/2003	JAPAN			Abstract	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

	Korean Office action for Korean patent application No. 10-2003-0007288 issued on 20 April 2005.

EXAMINER:	*DATE CONSIDERED:*

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP §609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.